A Low Jitter DLL-based Pulsewidth Control Loop With Wide Duty Cycle Adjustment

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Abstract—A pulsewidth control loop (PWCL) based on a delay-locked loop (DLL) is presented in the paper. The duty cycle of the proposed PWCL can be adjusted from 10% to 90% in 10% step. The circuit is designed and simulated using tsmc 0.13µm CMOS process. The operation frequency range is from 770MHz to 1.43GHz. The locking time of DLL is less than 15ns within the operation frequency band. The power dissipation is 3mW at 1.2V voltage supply. The peak-to-peak jitter is less than 2ps at an input clock frequency of 1.25GHz while adjusting various duty cycles.

I. INTRODUCTION

Pulsewidth control loops (PWCLs) based on phase-locked loops (PLLs) or delay-locked loops (DLLs) are used in applications such as the generation of the multiphase clock signals. In clock generation systems, it is important to have the duty cycles of the clock signals controlled accurately. The purposes of precisely controlled duty cycles are to synchronize the clock signals and to enhance the stability.

A conventional PWCL consists of a pulse generator, an odd-stage clock driver, a loop filter, and a comparator with two charge pumps [1][2]. The duty cycles of the clock signal are controlled by varying the time-delay of the odd-stage buffers in the multistage clock driver. Hence, the duty cycle adjustment is severely limited by the characteristics of the buffer stages if the sizes of the transistors are fixed.

The single-path PWCL shown in Fig.1 was designed with a built-in DLL [3]. Because the single-path PWCL provides a feedback path, PWCL and DLL can achieve the phase-locking at the same time so as to improve the performance. The duty cycle of the output signals can be tuned from 35% to 70%. However, the jitter of the DLL-based PWCL is not acceptable. It is desirable to have a simple PWCL circuit with both wide duty-cycle tuning range and low jitter performance.

II. PROPOSED PWCL ARCHITECTURE

The block diagram of the proposed DLL-based PWCL is shown in Fig. 2. The proposed PWCL consists of a phase detector (PD), a charge pump (CP), a loop filter (LP), a voltage-controlled-delay-line (VCDL), a half-transparent (HT) circuit, and switches. The PWCL products correct signals through comparing the input signal with the output signal of VCDL vcdl_clk.

Figure 1. Single-path PWCL with built-in delay-locked loop [3].

Figure 2. Proposed PWCL architecture.
Fig. 3 shows the timing diagram of the proposed PWCL. The half-transparent (HT) generates pulses which duty-cycle decides between two input signal positive edges. One of the input signals is ref_clk. The other is output signal of VCDL which is a multiphase clock signal. The voltage-controlled-delay-line produces alignment phase with sharing out ten equal parts. The switches connecting between the input of HT and the output of voltage-controlled-delay-line control the input of the HT. While the pulselength of 30% duty cycle is required, the switch controlled by $\Phi_3$ is closed. The HT can adjust the phases which are from ref_clk and $\Phi_3$ and provide the output signal. By switching the signals of VCDL, there are several different clock signals providing HT, and the output signal can suggest 10 different types of signal. The building blocks of the proposed DLL-based PWCL are described as follows.

A. Phase detector (PD)

In Fig. 4(a), the phase detector is a positive-edge clock trigger of ref_clk and vcdl_clk. PD consists of two half-transparent (HT) circuit as shown in Fig. 4(b). If the phase detector has a wide dead zone, it would result in a large jitter. In order to achieve time faithfully, the dynamic logic PD is used. Hence, HT of a true single-phase clock (TSPC) circuit can be operated in high frequency band easily.

B. Voltage Control Delay Line (VCDL)

In Fig. 5, the delay line consists of 10 delay cells. Each delay cell is composed of two current-starving inverters and their bias stages. The current-starving inverters are simple CMOS inverters whose delay time is varied through the output voltage of the charge pump.

C. Half-Transparent Circuit

HT circuit in the proposed PWCL is the same circuit as that used in PD only with different sizes of transistors. It is added for pulselength detection. After comparing the phase of ref_clk, different pulselength can be obtained. HT will be triggered when a positive clock edge of the clock signal is input as shown in Fig. 6.

D. CP and LP

CP and LP are parts of the built-in DLL. The schematics of CP and LP are shown in Fig. 7. After the phase detector produce UP/DN signal, the charge pump controls the charging or discharging current by UP or DN signal from PD. And then, the loop filter converts the charging/discharging current into the control voltage for driving different delay time of the delay line.
III. STABILITY ANALYSIS

The proposed PWCL is a one-pole system. Hence, only DLL is considered in the stability analysis. DLL in PWCL is a closed-loop system which includes a phase detector, a charge pump, a loop filter, and a voltage-controlled-delay-line. Fig. 8 shows the s-domain representation of the proposed PWCL in terms of DLL. \( D_{IN}(s) \) and \( D_{OUT}(s) \) represent the input and output clock signals of DLL, respectively. The transfer function can be expressed as

\[
H(s) = \frac{D_{OUT}(s)}{D_{IN}(s)} = \frac{F_{REF}I_{P}K_{VCDL}}{sC_{L}},
\]

where \( F_{REF} \) is the clock frequency of DLL, \( I_{P} \) is the current of the charge pump, and \( K_{VCDL} \) is the gain of the voltage-controlled-delay-line. In one-pole system, there is only one capacitor which results in advantages such as fast locked time and small chip area. The feedback circuit will not be affected by the switches and HT because the signals are transmitted to the output port directly. Hence, PWCL remains stable.

IV. SIMULATION RESULT

The proposed PWCL is designed with the tsmc 0.13\mu m CMOS process with the supply voltage 1.2V. The operating frequency of the input clock is from 770MHz to 1.43GHz. Fig. 9 and Fig. 10 show that the proposed PWCL can generate different duty cycles of output signals both at 770MHz and at 1.43GHz, respectively. The locked time of DLL is less than 10 cycles at 770MHz in Fig. 11. As depicted in Fig. 12, the peak-to-peak jitter is 2ps at 1GHz. Table I gives the performance summary of the proposed PWCL and the characteristics of other published PWCLs.

V. CONCLUSION

A wide duty cycle tuning range pulsewidth control loop based on a delay-locked loop is proposed. The duty cycle of the proposed PWCL can be adjusted from 10% to 90% in 10% step. The locking time of DLL is less than 15ns. The operation frequency range is from 770MHz to 1.43GHz. The power dissipation is 3mW at 1.2V voltage supply. The peak-to-peak jitter among 10%-90% adjustable duty cycle range is less than 2ps at an input clock frequency of 1.25GHz. The proposed low power pulsewidth control loop with low jitter performance is suitable for the clock generation systems.

VI. ACKNOWLEDGMENT

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TABLE I. PERFORMANCE COMPARISONS OF PWCLs

<table>
<thead>
<tr>
<th></th>
<th>This Work</th>
<th>[3]</th>
<th>[6]</th>
<th>[7]</th>
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<tr>
<td>CMOS Process (µm)</td>
<td>0.13</td>
<td>0.35</td>
<td>0.18</td>
<td>0.35</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
<td>3.3</td>
<td>1.8</td>
<td>3.3</td>
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<tr>
<td>Locked Time (ns)</td>
<td>&lt; 10</td>
<td>N/A</td>
<td>&lt; 600</td>
<td>28 cycles</td>
</tr>
<tr>
<td>Operating Frequency (GHz)</td>
<td>0.77 – 1.43</td>
<td>1 - 1.27</td>
<td>1 – 1.3</td>
<td>0.4 – 0.6</td>
</tr>
<tr>
<td>Duty Cycle (%)</td>
<td>10 – 90 @ 10%</td>
<td>35 – 70</td>
<td>30 – 70 @ 5%</td>
<td>30 – 70 @ 10%</td>
</tr>
<tr>
<td>Peak-to-peak Jitter (ps)</td>
<td>2 @ 1.25GHz</td>
<td>19.6</td>
<td>13.2 @ 1.3GHz</td>
<td>16.7 @ 500MHz</td>
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<tr>
<td>Power Consumption (mW)</td>
<td>3 @ 1.25GHz</td>
<td>150</td>
<td>4.8 @ 1.3GHz</td>
<td>20 @ 500MHz</td>
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VII. REFERENCES


