A CMOS 2.4GHz Delay-Locked Loop Based Programmable Frequency Multiplier

Ro-Min Weng, Tung-Hui Su, and Chuan-Yu Liu

Abstract—A CMOS delay-locked loop based frequency multiplier is presented. The multiplication factor N/2 can be chosen according to the number of the delay cell and the cascade stage of the multiplier sub-circuit. The output frequency range is from 270MHz to 2.4GHz using tsmc 0.18μm CMOS process parameters. The power consumption is 4mW with a 1.8V supply. The locking time of the DLL core is 1.78μs at 270MHz and 0.77μs at 400MHz. The phase errors are 43.44ps at 270MHz and 19.55ps at 400MHz. The cycle-to-cycle jitter of the DLL core is 8.29 ps.

I. INTRODUCTION

The problems in the distribution of unity clock signals throughout the entire high-speed systems are encountered. Thus it is required for an on-chip clock generator of multiple frequencies to be used in the high-speed system. Both the phase-locked loops (PLLs) and the delay-locked loops (DLLs) have been employed for the frequency synthesizers to generate the clock signals. DLLs are preferred for their unconditional stability and faster locking time than PLLs. Also the noise injected into a DLL disappears at the end of the delay line, whereas it is recirculated in an oscillator. DLLs are considered more suitable for multiple frequency synthesizer applications since they provide lower jitter than PLLs.

A DLL-based local oscillator has used an edge combiner for frequency multiplication [1]. However, it requires an LC tank, which occupies a large chip area. Also, the frequency multiplication ratio is fixed once the LC-tank component values are chosen. In [2], latches are used for frequency multiplication in a programmable DLL-based frequency multiplier. Since digital logic gates are sensitive to power supply noise, they significantly affect the peak-to-peak jitter performance of the frequency multiplier.

II. DLL-BASED FREQUENCY MULTIPLIER

The proposed CMOS DLL-based frequency multiplier in Fig.1 consists of four major blocks: a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), and a voltage-controlled delay line (VCDL). The reference clock (ref clk) is propagated through VCDL. The output signal (vcdl_clk) at the end of the delay line is compared with ref clk. If the delay which differs from the integer multiples of the clock periods is detected, the close loop will automatically correct it by changing the delay time of VCDL. In order to avoid the unlocking problem, the delay time of VCDL (T_{VCDL}) must have both the minimum and the maximum boundaries between the periods of ref clk. The VCDL outputs are level shifted to CMOS levels by a high gain buffer (two cascaded

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performance better than the fully differential delay lines. VCDL has no DC power dissipation using CMOS inverters.

D. Frequency Multiplier

Fig. 2 shows the proposed CMOS delay-locked loop based frequency multiplier. \( N \) input clocks feed to the multiplier to generate the frequency-multiplied output clock signal. \( c_{\text{clk}} \) signals are buffered from the VCDL outputs. The multiplier sub-circuit can be implemented by a composed CMOS inverter [5]. At the falling edge of \( c_{\text{clk}} \), both PMOS transistors are turned on for a short duration \( t_p \) and then transfer data to the output when the output goes high. The output goes low at the rising edge of \( c_{\text{clk}} \). Thus, output clock signal toggles at every rising and falling edge of \( c_{\text{clk}} \). The programmable phase selection circuit overcomes the fixed frequency multiplication ratio problem. 12-stage delay elements and cascade 6-stage of multiplier sub-circuit are employed to implement multiple-by-6 output clock frequency. Six pairs of phases, \((c_{\text{clk}1}, c_{\text{clk}2}), (c_{\text{clk}3}, c_{\text{clk}4}), (c_{\text{clk}5}, c_{\text{clk}6}), (c_{\text{clk}7}, c_{\text{clk}8}), (c_{\text{clk}9}, c_{\text{clk}10})\), and \((c_{\text{clk}11}, c_{\text{clk}12})\) are selected. The buffer drives a large output capacitive load. As shown in Fig. 3, multiple-by-3 frequency is achieved. VCDL generates 6 signal phases, and employs 3-stage frequency multiplier sub-circuits. Three pairs of phases \((c_{\text{clk}1}, c_{\text{clk}1}), (c_{\text{clk}2}, c_{\text{clk}2}), (c_{\text{clk}3}, c_{\text{clk}3}), (c_{\text{clk}4}, c_{\text{clk}4}), (c_{\text{clk}5}, c_{\text{clk}5}), (c_{\text{clk}6}, c_{\text{clk}6}), (c_{\text{clk}7}, c_{\text{clk}7}), (c_{\text{clk}8}, c_{\text{clk}8})\), and \((c_{\text{clk}9}, c_{\text{clk}9})\) are selected and feed to 3-stage frequency multiplier sub-circuits. Multiplication factor \( N/2 \) can be chosen according to the number of delay elements and the programmable phase selection circuit in Fig.4.

IV. SIMULATION RESULTS

The proposed circuit is simulated using tsmc 0.18\( \mu \)m CMOS process parameters with a 1.8V supply voltage. The locking time and the static phase error are simulated at 270 MHz input reference clock as shown in Fig. 5(a) and 5(b), respectively. The proposed frequency multiplier can correctly multiple the output clock frequency depending on the phases average distribution. Fig. 6 shows the output multiple-by-3 frequency waveform at 400 MHz input reference clock. The simulation results are listed in Table I.

![Fig. 2. Proposed frequency multiplier.](image)

![Fig. 3. Waveform of the multiple-by-3 output frequency.](image)

![Fig. 4. Programmable frequency multiplier.](image)

V. CONCLUSIONS

The proposed CMOS DLL-based frequency multiplier can multiply the frequency of input signal without a jitter accumulation problem. Multiplication factor can be chosen according to the number of delay cell and the cascade stage of the multiplier sub-circuit. The output frequency range can be obtained from 270MHz to 2.4GHz. The power consumption is 4mW with a 1.8V supply. The locking time of the DLL core is 1.78\( \mu \)s at 270MHz and 0.77\( \mu \)s at 400MHz. The phase errors are 43.44ps at 270MHz and 19.55ps at 400MHz. The cycle-to-cycle jitter is 8.29ps. The proposed circuit is suitable for high-speed systems due to the advantages of low power, multiple output frequencies, fast locking and low phase error.

REFERENCES


![Fig. 5. (a) Locking time (b) static phase error at \( f_o=270\text{MHz} \).](image)

![Fig. 6. Output multiple-by-3 frequency waveform at \( f_o=400\text{MHz} \).](image)

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